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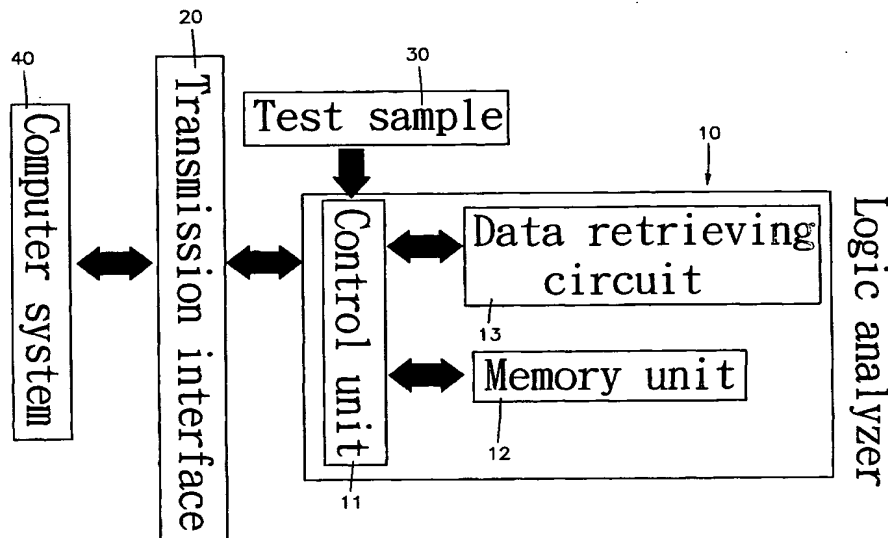
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(54) Title: LOGIC ANALYZER DATA RETRIEVING CIRCUIT AND ITS RETRIEVING METHOD



(57) Abstract: A logic analyzer data retrieving method used in a logic analyzer formed of a control unit (11), a memory unit (12), and a data retrieving circuit (13), is disclosed to include the step of driving the data retrieving circuit of the logic analyzer to receive a time delay default value and to store in a buffer in a time delay circuit, and the step of triggering the preset of a first counter and transferring the default value from the buffer to the first counter to drive the first counter to start counting when a clock qualifier signal entered so as to obtain a complete clock enable signal when the first counter counted up to the default value and the output of the clock enable became low.